IN THE SPECIFICATION:

Please replace paragraph **[0006]** with the following:

A1

[0006] If the interposer is positioned adjacent the active surface of the semiconductor die, the bond pads of the semiconductor die may be electrically connected to corresponding contact areas on an opposite, top surface of the interposer by way of intermediate conductive elements that extend through one or more holes formed in the interposer. Again, the contact areas communicate with corresponding bumped contact pads on the interposer. In this type of flip-chip semiconductor device assembly, however, the contact pads are also typically located on the top surface of the interposer. Accordingly, this type of flip-chip assembly is positioned adjacent a carrier substrate by orienting the interposer with the top surface thereof facing the carrier substrate.

Please replace paragraph **[0010]** with the following:

A2

[0010] Another approach to reducing the sizes of assemblies of semiconductor devices and carrier substrates has been to reduce the amount of "real estate", or surface area, upon a carrier substrate that is consumed by individual semiconductor device packages. This is typically done by reducing the dimensions of the semiconductor device packages along a plane that is parallel to a plane of the substrate upon which the semiconductor device packages are to be carried. As a result of ever-decreasing package dimensions, the so-called "chip-scale package" (CSP) has been developed. The dimensions of the outer peripheries of chip-scale packages are typically substantially the same as or only slightly larger than the corresponding dimensions of the outer peripheries of the semiconductor dice that are used in chip-scale packages.

Please replace paragraph **[0011]** with the following:

A3

[0011] As indicated previously herein, some chip-scale packages have ball grid array connection patterns. Some ball grid array chip-scale packages include interposers that are configured to be secured over the active surfaces of semiconductor dice, with bond pads of the

dice being exposed through an opening formed through the interposer. Due to the limited dimensions of chip-scale packages, the dimensions of the interposers for use therein are also constrained, as are the sizes of openings formed through the interposers. In addition, state of the art semiconductor dice typically include bond pads that are positioned very near the outer peripheries of the dice. Consequently, in order to maintain the structural integrity of chip-scale package interposers, the interposer openings may not extend a sufficient lateral distance beyond bond pads of their corresponding semiconductor devices to provide adequate clearance for the tip of a wire bonding capillary or other intermediate conductive element-forming, -positioning, or -securing apparatus to properly access the bond pads.

Please replace paragraph **[0014]** with the following:

A4

[0014] The interposer of the present invention includes a substantially planar substrate element that may be formed from any suitable material, such as resin (e.g., FR-4 resin), plastic, insulator-coated semiconductor material (e.g., silicon oxide-coated silicon), glass, ceramic, or any other suitable electrically insulative material or insulative-coated material. The interposer also includes an opening, or slot, formed therethrough. The slot is positioned to be aligned over the bond pads of a semiconductor die upon mutual positioning of the interposer and the semiconductor die. Thus, when the interposer and semiconductor die are properly oriented, the bond pads of the semiconductor die are exposed through the slot of the interposer.

Please replace paragraph **[0016]** with the following:

A5

[0016] A semiconductor device package incorporating teachings of the present invention includes a semiconductor die, an interposer positioned over an active surface of the semiconductor die, wire bonds connecting bond pads of the semiconductor die to corresponding contact areas of the interposer, and a quantity of encapsulant material at least partially filling the slot formed through the interposer and at least partially covering the active surface of the semiconductor die. The encapsulant material may also extend at least partially onto the surface

of the interposer and above the surface of the interposer to substantially encapsulate the bond wires that connect bond pads of the semiconductor die to corresponding contact areas of the interposer.

Please replace paragraph **[0018]** with the following:

[0018] While the foregoing exemplary methods may be used to form a slot with a laterally recessed area at a portion of an end thereof on any type of substrate element, including, without limitation, a resin, a plastic, dielectric-coated silicon (*e.g.,* silicon oxide-coated silicon), glass, ceramic and other suitable insulative or insulator-coated substrate elements, slots having a laterally recessed area formed in only a portion of a periphery (*e.g.,* at an end) thereof may be formed by other suitable techniques. For example, if the substrate element of the interposer is formed from silicon or another etchable material, such as glass or ceramic, known patterning processes, such as the use of known masks and etchants, which are typically used in semiconductor device fabrication processes may be employed to define a slot in the substrate element, as well as a laterally recessed area in a peripheral edge of the slot.

Please replace paragraph **[0027]** with the following:

[0027] Although it has many applications in semiconductor die packaging, an interposer or another substrate element of the present invention may best be described in relation to a board-on-chip assembly. A semiconductor device assembly 10 incorporating teachings of the present invention, as shown in FIGs. 1 and 2, has conductive structures 46 (shown in FIG. 5) (*e.g.*, balls, bumps, or pillars of solder, another metal or metal alloy, or z-axis conductive elastomer) protruding therefrom in a ball grid array connection pattern and includes a semiconductor die 20 and a substrate element, which is also referred to herein as an interposer 30.

Please replace paragraph **[0028]** with the following:

A8

[0028] The interposer 30 includes a substantially planar substrate element 31 that may be formed from any suitable material, such as resin (e.g., FR-4 resin), plastic, insulator-coated semiconductor material (*e.g.,* silicon oxide-coated silicon), glass, ceramic, or any other suitable, electrically insulative or at least partially dielectric-coated material, and may be positioned over the active surface 22 of the semiconductor die 20.

Please replace paragraph **[0029]** with the following:

A9

[0029] As shown, the interposer 30 includes an aperture, or slot 14, formed therethrough for exposing the bond pads 12 of a semiconductor device 20 over which the interposer 30 is to be positioned. The slot 14 has a first end 15 that is configured to extend laterally beyond an outer periphery 21 of the semiconductor die 20 when the interposer 30 and semiconductor die 20 are properly oriented with respect to one another. As the first end 15 of the slot 14 is configured to extend beyond the outer periphery 21 of a semiconductor die 20 to which the interposer 30 is attached, the first end 15 does not restrict the flow of encapsulant material being introduced into the slot 14 and is, therefore, also referred to herein as a "nonmold flow restriction end".

Please replace paragraph **[0030]** with the following:

A10

[0030] Another end 16 of the slot 14, which may be located opposite the first end 15, includes a laterally recessed area 17 in a peripheral edge 18 of the slot 14. The laterally recessed area 17 provides additional lateral access to a bond pad 12 located at or near the outer periphery 21 of the semiconductor die 20. Specifically, the laterally recessed area 17 provides additional access to bond pad 12E (see FIG. 4) that is located adjacent an outer periphery 21 of the semiconductor die 20, which is also referred to herein as an end bond pad, at a location between the bond pad 12E and the adjacent portion of the outer periphery 21 of the semiconductor die 20, than would otherwise be available with a chip-scale package interposer. As shown, the laterally recessed area 17 of slot 14 may extend beyond the outer periphery 21 of

the semiconductor die 20 when the interposer 30 and the semiconductor die 20 are properly oriented with respect to one another. By providing an additional lateral opening around a portion of the end bond pad 12E, the laterally recessed area 17 may facilitate access to the end bond pad 12E by equipment that forms or positions intermediate conductive elements 43 on bond pads 12 (*e.g.*, a portion of a wire bonding capillary).

Please replace paragraph **[0032]** with the following:

[0032] Contact areas 34 are carried upon a top surface 32 of the interposer 30. Preferably, the contact areas 34 are located proximate the slot 14 so as to facilitate the positioning of relatively short intermediate conductive elements 43 through the slot 14, between the bond pads 12 of a semiconductor die 20 and the contact areas 34. As illustrated in FIGs. 1 and 2, a circuit trace 36 extends laterally from each contact area 34 to a corresponding terminal 38, which may also be carried upon the top surface 32 of the interposer 30, electrically connecting each contact area 34 to its corresponding terminal 38.

Please replace paragraph **[0033]** with the following:

[0033] To arrive at a board-on-chip configuration, such as that illustrated in FIGs. 1 and 2, a semiconductor die 20 is placed below each slot 14 in a die attach or die-receiving area of the interposer 30 so as to be positioned underneath the interposer 30 with bond pads 12 of the semiconductor die 20 being exposed through the slot 14. An active surface 22 of the semiconductor die 20 faces a backside 33 of the interposer 30 and may be secured thereto via a quantity of adhesive material 40.

Please replace paragraph **[0041]** with the following:

[0041] Alternatively, with reference to FIGs. 7 and 7A, the slot 14 and the laterally recessed area 17 thereof may be formed by using a drill 80 and a first drill bit 81 to form a first, small hole 74 through the substantially planar substrate element 31 at areas thereof where the

slot 14 and the laterally recessed area 17 are to be located. As shown in FIG. 7, the first, small hole 74 may be formed by allowing the first drill bit 81 to penetrate the substantially planar substrate element 31 and, while the first drill bit 81 is being rotated and continues to intersect the plane of the substantially planar substrate element 31, by moving the first drill bit 81 in a direction parallel to the plane of the substantially planar substrate element 31.

Please replace paragraph **[0042]** with the following:

[0042] FIG. 7A depicts the introduction of a second drill bit 82 into the first, small hole 74. The second drill bit 82 has a larger diameter than that of the first drill bit 81 (FIG. 7). The first, small hole 74 serves as a guide to the second drill bit 82 as the second drill bit 82 is moved along the first, small hole 74 in a direction parallel to the plane of the substantially planar substrate element 31 to increase the thickness of the first small hole 74 and to form a second, wider hole 76 at locations where the slot 14 is to be located. Stated another way, the second drill bit 82 is used to form the second hole by increasing the width of the first, small hole 74 at all locations along the length thereof except for that at which the laterally recessed area 17 is to be located. The laterally recessed area 17 is formed by the remaining, original width portion of the first, small hole 74.

Please replace paragraph **[0045]** with the following:

[0045] In forming semiconductor device assemblies 10, a quantity of a suitable adhesive material 40 is applied to at least portions of one or both of the backside 33 of each interposer 30 and the active surface 22 of each semiconductor die 20. Known processes, including, without limitation, spray coating, curtain coating, use of a doctor blade, or positioning of a film or tape bearing adhesive material 40 on both major surfaces thereof, may be used to apply the adhesive material 40 to the backside 33 of the interposer 30, to the active surface 22 of the semiconductor die 20, or to both backside 33 and active surface 22. The adhesive material 40

is preferably positioned such that it will not cover the bond pads 12 of a semiconductor die 20 once the interposer 30 and semiconductor die 20 are assembled.

Please replace paragraph **[0046]** with the following:

[0046] With reference to FIG. 4, a semiconductor die 20 may then be positioned relative to and secured to each interposer 30 on the strip 50 to form semiconductor device assemblies 10 that are physically connected to one another by way of the material that physically connects adjacent interposers 30 along the strip 50. When each semiconductor die 20 is properly positioned relative to an interposer 30 on the strip 50, the bond pads 12 of the semiconductor die 20 will be exposed through both the adhesive material 40 (FIG. 3) and the slot 14 formed through the interposer 30. The laterally recessed area 17 of the slot 14 of each interposer 30 is positioned laterally adjacent to a bond pad 12E that is located adjacent an outer periphery 21 of the semiconductor die 20.

Please replace paragraph **[0048]** with the following:

[0048] Turning now to FIG. 5, at least a portion of the active surface 22 of each semiconductor die 20 may also be encapsulated, as known in the art, by introducing a quantity of a suitable encapsulant material 45 (*e.g.*, a filled polymer transfer molding compound or a silicone or epoxy glob-top type encapsulant material) into the slot 14. The encapsulant material 45 preferably covers at least portions of the active surface 22 of the semiconductor die 20, including the bond pads 12 thereon. The encapsulant material 45 may also substantially cover the intermediate conductive elements 43 that extend between the bond pads 12 of each semiconductor die 20 and the corresponding contact areas 34 of the interposer 30. Accordingly, the encapsulant material 45 may substantially fill the slot 14 and cover the regions of the top surface 32 of the interposer 30 at which the contact areas 34 are located.

Please replace paragraph **[0050]** with the following:

A18

[0050] Conductive structures 46, such as balls, bumps, or pillars formed from a conductive material, such as solder, another metal or metal alloy, or z-axis conductive elastomer, may be secured to terminals 38 (FIGs. 1-2) of the interposer 30 to facilitate the connection of semiconductor device assembly 10 to a carrier substrate or to another assembly, such as in a multi-chip module (MCM) configuration, as known in the art.

Please replace paragraph **[0051]**with the following:

A19

[0051] Adjacent semiconductor device assemblies 10 may be separated from one another by use of known processes, such as by saw-cutting or use of an energy beam (*e.g.,* a laser or ion beam) to cut the strip 50 at locations between adjacent interposers 30.

Please replace paragraph **[0052]** with the following:

A20

[0052] Of course, semiconductor device assemblies 10 may also be formed separately from one another by securing an individual interposer 30 and semiconductor die 20 to one another, as described previously herein with respect to FIG. 3, and electrically connecting the bond pads 12 of the semiconductor die 20 to corresponding contact areas 34 of the interposer 30.

Please replace paragraph **[0053]** with the following:

A21

[0053] As another alternative, semiconductor device assemblies 10 may be formed on a larger scale, such as a wafer scale, wherein an array of physically connected interposers 30 is provided (*e.g.,* on a wafer or other large-scale substrate) and semiconductor dice 20, which may be separate from one another or also physically connected to one another on a large-scale substrate, are aligned with and secured to the interposers 30.